Fault Site Localization Technique by Imaging with Nanoprobes

Takeshi Nokuo, JEOL Ltd., Japan
Hitoshi Furuya, Fujitsu Microelectronics Ltd., Japan
nokuo@jeol.co.jp

Introduction

In the semiconductor industry, progress in failure analysis (FA) is indispensable for improving the productivity of devices. However, recent aggressive downsizing of devices with multilayer structures complicates and diversifies failure modes, making FA extremely difficult. Engineers engaged in FA spend much more time in localizing fault sites; even worse, they are faced with cases where fault site localization is impossible. Therefore, to improve FA yield, which reveals the physical root cause of a faulty device and feeds it back to the process line, it is essential to implement new defect localization techniques that keep up with new technology development.

Nanoprobing techniques have been developed to meet these demands. The nanoprobing method with a scanning electron microscope (SEM) achieves higher spatial resolution than the former probing method with an optical microscope. This new method facilitates fault site localization down to an individual transistor level, which cannot be achieved by the former method.

Unlike the optical beam of a former probing method, interactions of the focused electron beam of an SEM and a device generate electron beam induced current (EBIC) and absorbed electrons (AEs). Research on EBIC in devices started in the 1950s, and a few examples of the usefulness of EBIC for FA were reported in 1980.[1] The principle of EBIC is that electron-hole pairs generated by primary electron irradiation drift along in an internal electric field near p-n junctions in a device to produce an electric current. This makes a device under observation act as a detector of electric current, and EBIC directly represents the local electronic states of the device, which gives valuable information for FA. Unfortunately, however, EBIC has not been used for FA of actual very large-scale integrated (VLSI) circuits until quite recently. The reason is that EBIC generated near the target site is difficult to extract because it flows along a complicated current path in a VLSI circuit. Recent implementation of nanoprobing, however, overcomes this “old” limitation of EBIC detection in VLSI circuits. Internal probing gives a direct path for EBIC, which can be detected to produce an image for FA.

Methods of detecting AEs have also been studied for years as a part of research on EBIC.[2] The physical...
The principle behind AE generation is the diffusive motion of stay-in charge carriers, which are the difference between injected charge carriers by incident electrons and emissive charge carriers such as secondary electrons, to maintain charge neutrality in a device. A remarkable report on the application of AE detection to FA was published in 1986 as resistive contrast imaging (RCI).[3] The RCI method is also used by internal probing, which enables direct detection of signals from any very small area in a device, for making images to visualize defects.[4]

In this paper, a method for using an SEM-based nanoprobe system for EBIC/AE observation is explained,[5] and a few FA examples are presented.

**EBIC Detection by Nanoprobes**

Figures 1(a) and 1(b) show schematic illustrations of planar and cross-sectional EBIC observation by nanoprobes. Contrast of an EBIC image is associated with the internal electric field near a $p$-$n$ junction, so that EBIC is generally used to evaluate the diffusion region. In the case of the planar EBIC observation, when primary electrons are accelerated at a high enough voltage to penetrate into the diffusion region, a direct contact to an interconnect layer can be attained. The planar EBIC observation gives a two-dimensional shape, including uniformity of the diffusion region, as shown in Fig. 2(a). Cross-sectional observation indicates the site of the depletion region, as shown in Fig. 2(b). When the IV converter is switched to a voltage amplifier, electron beam induced voltage can be observed.

The principles of absorbed electron imaging (AEI) and voltage distribution contrast (VDIC)[6] are shown schematically in Fig. 3(a) and (b), respectively. In AEI, both ends of a target interconnect are nanoprobe;
one connects to a ground potential and the other to the IV converter. Displaying gray scale according to detected AEs by the IV converter at each irradiation point creates AEI. When primary electrons are irradiated between groundside and a high-resistance site, AEs, which are generated at each irradiation point, distribute to groundside, so the IV converter detects a small amount of AEs. However, when primary electrons pass across the high-resistance site, most of the AEs distribute to the IV converter, which has low input impedance, and the IV converter detects higher AEs. As a result, the contrast of AEI suddenly changes at a high-resistance site, and the fault site can be recognized as a boundary of the contrast on AEI.

A VDIC configuration is almost the same as AEI, except for the use of a voltage amplifier, which has extremely high input impedance, rather than an IV converter. When primary electrons are irradiated on all interconnect sites, AEs, which are generated at each irradiation point, distribute to groundside. In between groundside and the high-resistance site, the AEs generate a small voltage because the resistance of this area is relatively small. When primary electrons pass across the high-resistance site, AEs create higher voltage because of the high-resistance site; these voltages are detected by the voltage amplifier. Therefore, the contrast of VDIC suddenly changes at a high-resistance site, and the fault site can be recognized as a boundary of the contrast.

AEI and VDIC are based on AE generation, so these methods are mainly employed for interconnect analysis. AEI has an advantage in detecting a fault site with relatively high resistance, whereas VDIC is better for detecting those with relatively low resistance. These two methods are also useful for detecting short-circuit sites, as shown in Fig. 4.

**Role of Nanoprobes in the FA Process**

The fault site localization process is generally performed as follows:

- Select a larger candidate area surrounding the fault and then narrow it down to a smaller area, step by step, based on data provided by software tools or hardware analysis instruments, finally localizing a specified element with the fault area.

- An SEM-based nanoprobing system is used in the last step of the process, that is, precise identification of the fault site to reveal a physical root cause of the failure.

In the first step, a large candidate area around the fault is typically estimated with the data provided by software tools, such as software diagnosis tools for logic device or fail bit map (FBM) for memories, and/or with the data from hardware instruments, such as an emission microscope and optical beam induced resistance change (OBIRCH). After these processes, nanoprobes, which are able to use the submicron-scale electrical properties EBIC and AEI, can efficiently and accurately determine the site of unusual ion implantation or a small current path, which have been less successfully identified in recent devices.

**Fig. 4** Short-circuit site detection by AEI. (a) AEI of a reference device. (b) AEI of a faulty device. In (a), only one net is extracted by AEI. In (b), an additional net is extracted. In this case, the faulty device is assumed to have short-circuit failure, and the closest point between these two interconnects is defined as the most suspicious short-circuit site and is physically analyzed.
FA for Scan Failure of a Large-Scale Integrated Logic Circuit by AEI

At first, the fault phenomenon was reproduced and reconfirmed by tester-derived logic fault information. Then, based on this information, a software diagnosis tool extracted candidates for fault nets and layouts. As a result, candidate fault sites were widely patterned through the multilayer structure in the chip, so physical analyses of all these candidates were considered to be impossible. Hence, further localization was required. When a backside emission microscope was applied on this chip, an anomalous emission site was recognized around one of the candidates. By focusing on a specific interconnect that connected this anomalous emission site and the underlying circuit, AEI was applied. Figure 5(a) shows AEI of the target interconnect, and Fig. 5(b) shows a superimposed image of the AEI on the secondary electron image (SEI). Comparing these images with the layout diagram of this interconnect confirmed that the contrast of this interconnect-patterned lower layer disappeared in the middle. An output driver of this interconnect was located in the top-left part of Fig. 5(b), whereas an input poly gate was located at the other end. Therefore, an unstable input level to this circuit may cause anomalous emission by a pass-through current. Figure 6 shows an SEI of the site, where contrast of the AE disappeared abruptly after all upper layers were removed by deprocessing. An open site along this interconnect was clearly observed in this image.

FA for Memory Cell Array by AEI

A candidate fault site in this memory array was extracted by FBM, which suggested a line failure mode. This line was directly nanoprobed to an amplifier, and AEI was employed. Figure 7 shows an AEI of this interconnect. In this image, a target interconnect and one other interconnect patterned below the former one were visualized so that the fault site was confirmed to be located at the cross point of AEI, and the failure mode was a short circuit between these two lines. After AEI observation, more detailed physical analysis, such as layer-by-layer observation or cross-sectional imaging at the cross point, provides a reason for the short circuit, that is, a patterning or defect-caused failure.
The last example was a single bit failure (margin failure) of a memory cell. After a fault cell was extracted by FBM, the cell was observed layer by layer with an SEM to identify an interconnect failure. SEM voltage contrast was also performed to evaluate a contact via, but no fault site was recognized. After these processes, transistor characteristics were measured by nano-probes. As a result of an anomalous $V_g$-$I_d$ forward characteristic, $V_{th}$ of the PMOS transistor was shifted, and $I_{on}$ remained low. On the other hand, $V_g$-$I_d$ reverse characteristics of this PMOS transistor and $I_{on}$ were hardly affected. Figure 8 shows the forward and reverse $V_g$-$I_d$ characteristics of this PMOS transistor. Meanwhile, the $V_g$-$I_d$ characteristics of the next transistor, which shared the source region, were confirmed to be normal.

Judging from these PMOS characteristics, a failure mode was assumed to be a physical ion implantation failure, a shortage of ion implantation, and a marginal contact at the bottom of a contact via. To analyze more details, planar EBIC observation was performed on this device. Figure 9 shows the results of the EBIC observation.
analyses. In the case of the faulty PMOS transistor, EBIC contrast from the drain region appeared relatively smaller and weaker than those of the reference PMOS transistor. Also, a cross-sectional EBIC image of this region is shown in Fig. 10. EBIC contrast around the target drain area was smaller and weaker, similar to the planar observation. EBIC contrast is associated with a difference in carrier pair generation rate or in concentration of ionized dopants, so an error in the ion implantation process for the diffusion region was assumed to raise the resistance. However, spatial resolution in an EBIC image at this moment is not high enough to identify the process that caused this phenomenon, so a simulation study was performed to clarify a physical root cause based on electrical characteristics. After applying several conditions, when ion implantation was processed with a particle or a resist defect remaining on a gate sidewall, electrical characteristics similar to the faulty bit were obtained. A model and the result of the simulation are shown in Fig. 11 and 12, respectively.

In this study for a single bit failure (PMOS transistor failure) of a memory cell, a physical root cause and a suspicious process were revealed by using electrical characteristics measurement with nanoprobes, fault site visualization with nanoprobe EBIC, and an estimation of the failure mechanism with a simulation study.

Conclusions

Improvements of innovative processes through application of advanced technology and increases in yield of new products with larger scale integration strongly depend on FA. Recent downsizing of devices, however, makes the localization of fault sites impossible by the former FA techniques. As reported in this paper, an SEM-based nanoprobe system has made it possible to measure electrical properties, EBIC and AEI, from areas as small as the submicron range. Measurement and imaging with this instrument expands the former limit of fault site localization down to a submicron range, which helps substantially in clarifying physical root causes leading to faults. The authors believe that the technique will be an indispensable tool in the field of FA.

References

Fault Site Localization Technique by Imaging with Nanoprobes
(continued)


About the Authors

Takeshi Nokuo began his career at JEOL in 1990 as a research and development engineer, mainly engaging in the development of scanning electron microscopes and their applications. Since 2004, he has been developing new failure analysis techniques using nanoprobing.

Hitoshi Furuya joined the Quality Assurance Group of the Semiconductor Business unit at Fujitsu Ltd. in 1991. He works on system LSI failure analysis at the Fujitsu Microelectronics Mie factory. His interest is currently focused on the use of the electron beam for new technology development in failure analysis.

Noteworthy Item

Free Online Access to 12 Journals Now Available to EDFAS Members

ASM International and EDFAS are pleased to offer even more value to members without raising membership dues! As a member of EDFAS, you’re now entitled to full-text online access to two of the most respected journals in the materials field—Metallurgical and Materials Transactions A&B—as well as ten other highly respected Springer-owned journals:

- Journal of Materials Science
- Journal of Materials Science: Materials in Electronics
- Journal of Materials Science: Materials in Medicine
- Applied Physics A: Materials Science and Processing
- International Journal of Fracture
- Journal of Non-Destructive Evaluation
- International Journal of Mechanics of Materials in Design
- Metal Science and Heat Treatment
- Oxidation of Metals
- Tribology Letters

As a member benefit, EDFAS members can access the full text of all articles in Metallurgical and Materials Transactions A&B, going back to the first issue in 1970, online at SpringerLink. Backfiles of the Springer-owned journals are also available. Please follow these steps to access your online content:

1. Go to the EDFAS website at www.edfas.org and log in as a member.
2. On the “My EDFAS” page, scroll down to “My Community.”
3. Under “My Personal Subscriptions,” click on “Technical Journals.” This will take you to the Members-Only journals page on the ASM website.

4. Select “Read Online” to access your active member subscriptions. For EDFAS and ASM members, these include the two Met. Trans. journals plus the ten Springer-owned journals listed at the bottom of the page. (The other ASM journals listed are available by subscription at a special reduced price for members.) This will take you directly to the journal content on SpringerLink. No further entry of user name or password will be needed.

Any journals to which you are not a member subscriber (or receive free access by virtue of ASM/EDFAS membership) will default to a “Subscribe Now” link. If you click this link, you will be given an opportunity to begin a new subscription to this journal at the special ASM member rate through an online form on Springer’s website.

Please note that if you have recently been to the Springer site other than through ASM, it may remember you as a nonsubscriber. If that happens, you may need to clear out the cookies and temporary history files on your computer and close your internet connection. When you then go back in through the ASM site, it should recognize you as a subscriber. You should not be asked to log in on the Springer site at any point or to pay for access.

If you have any difficulties in reaching the Members-Only journals page or do not know your EDFAS user name and password, please contact Customer Service at customer.service@asminternational.org or 440/338-5151, ext. 0.